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Description

Bulk Contact Mask Process

Background of Invention

[0001] The field of the invention is that of integrated circuits containing DRAM arrays with closely-spaced trench capacitors.

[0002] In the field of trench DRAMS, workers are constantly striving to pack more cells in a given area. The use of a vertical transistor instead of a planar transistor was an important step in shrinking the transverse dimensions of the cells, though at the cost of the expensive etching process to form the deep trenches, now about 8 microns deep.

[0003] As those skilled in the art are aware, the vertical trench transistor has its gate formed in the trench and its body in a well (typically a P-well) formed in the bulk silicon.

[0004] At the bottom of the vertical transistor body, a buried strap, which is an N-type doped region of the substrate formed by outdiffusion from material inside the trench, creates a depletion region in the P-well. When the capacitor at the bottom of the cell is charged, the diffusion re-

gion increases in extent.

[0005] The dopant concentration in P-wells is low, in an attempt to reduce leakage of the charge stored in the cell capacitor. Unfortunately, the low dopant concentration increases the length of the depletion region.

[0006] The foregoing circumstance, together with the reduced distance between cells resulting from the increase in cell packing density has meant that the depletion regions from adjacent cells can overlap, effectively pinching off the transistor bodies above them.

[0007] This, in turn, means that the transistors have floating bodies and therefore suffer from the effects of those floating bodies, such as reduced drive, which, in turn, reduces the amount of charge stored in the capacitor.

[0008] It would be highly desirable to construct a DRAM that has increased packing density without the undesirable effects mentioned above.

SUMMARY OF INVENTION

[0009] The invention relates to a trench-capacitor, vertical transistor DRAM array that has an insulating structure placed between adjacent cells.

[0010] A feature of the invention is etching a set of trenches placed between DRAM cells and extending down below

the level of the buried straps in the DRAM cells.

[0011] Another feature of the invention is the blockage of a horizontal path between adjacent buried strap diffusions.

[0012] Another feature of the invention is the provision of a vertical conductive path from the level of the transistor bodies to below the buried strap diffusions.

Brief Description of Drawings

[0013] Figure 1 shows a cross section of a portion of a DRAM array, showing the close approach of buried strap outdiffusion regions.

[0014] Figure 2 shows an isolating trench etched into the region shown in Figure 1.

[0015] Figure 3 shows the isolating trench after deposition and recession of a nitride liner.

[0016] Figure 4 shows the region after deposition and recession of boron-doped poly to the level of the transistor bodies of the vertical cell transistors.

[0017] Figure 5 shows the completed structure, blocking horizontally and connecting vertically.

[0018] Figure 6 shows a top view of the layout of the trenches.

Detailed Description

[0019] Referring to Figure 6, there is shown a top view of a por-

tion of a DRAM array. Deep trenches (DT) 62 contain the capacitor and vertical transistor of the cell. Interconnections to bit lines and word lines will be added at a later time.

[0020] Between trenches 62, there are blocking / bulk contact trenches 65 that perform the dual functions of blocking the spread of depletion regions from the buried straps and also establishing a vertical conductive path extending from the transistor bodies down below the buried straps.

[0021] Trenches 62 are defined by a mask, referred to as the DT separation mask, that inevitable will not be perfectly aligned with the DT mask. There will, therefore, be a difference in distance between the vertical contact formed according to the invention and the body of the vertical transistors on the left and right. Preferably, the contact trenches are made as small as possible (having the minimum lithographic dimension available in the current process) so that the misalignment is a relatively small fraction of the total distance between trenches.

[0022] Figure 1 shows a cross section of a portion of the array perpendicular to line 1 - 1 of Figure 6. In this figure, two DRAM cells 100 are shown, with a capacitor 105 at the bottom of the trench, shown schematically by dotted line

105, and a vertical transistor placed above the capacitor. The capacitor 105 is only shown schematically in the drawing as its structure is conventional and not relevant to the practice of the present invention.

[0023] The portion of the semiconductor wafer (e.g. silicon) in which the transistors are located is a P-well 20, doped to a conventional concentration with p-type dopant. The bulk of the wafer is doped N-type, the transition between P-type and N-type being located below buried straps 120, at a height where collar oxide 112 insulates the capacitor from the bulk silicon.

[0024] The transistors are bounded vertically on the bottom by a buried strap 120 that forms the drain and on the top by a horizontal diffusion 122 that forms the source and also the contact to the bit line (added in a later step). Upper nitride spacers 127, together with the gate oxide, separate the transistor gate 125 from the source 122.

[0025] At the bottom of the trench, capacitor 105 has been formed with center electrode 110. At the level shown, electrode 110 is insulated from the bulk silicon by collar oxide 112. Above oxide 112, the material of the center electrode has formed the interior portion of the buried strap and diffused dopant into the bulk silicon to form

drain 120. Trench top oxide (TTO) 122 separates the center electrode from the transistor gate 125.

[0026] Drains 120 are separated by distance 11. Nominally, the horizontal extent of drains 120 is 1F, where F is the symbol for the minimum lithographic distance, nominally 100nm, say. In this case, distance 11 is also 1F, which is the amount allocated for the isolation trenches to be built.

[0027] Referring back to Figure 6, it can be seen that the trenches 210 have a width about equal to the separation from the adjacent deep trench, which is also the length of the drains (1F according to the example). Along 1 - 1 (vertical in Figure 6), the length is considerably longer, nominally 2x, to provide better overlap with the isolation trench area between the active area lines.

[0028] The overall process sequence may be summarized as: Form DRAM cells containing trench capacitors and vertical transistors connected by buried straps.

[0029] Etch through top oxide over the region between DRAM cells.

[0030] Form a second set of trenches (contact trenches) placed between DRAM cells and extending down below the buried strap depth (using a silicon etching process selective to oxide).

[0031] Form an oxide liner in the second set of trenches.

[0032] Form a nitride liner in the second set of trenches.

[0033] Reactive ion etch (RIE) the trenches directionally, removing the nitride and oxide liner on the bottom.

[0034] Fill the second trenches with resist; recess the resist.

[0035] Etch the exposed portion of the nitride spacer selective to oxide.

[0036] Perform nitridation on the upper portion above the nitride liner Deposit boron-doped poly in the trenches.

[0037] Recess the poly.

[0038] Diffuse boron into the P-well through the upper portion of the trench (above the nitride liner).

[0039] Fill the upper part of the trench with Nitride.

[0040] Oxide etch on the wafer surface, exposing the top of the DRAM cells.

[0041] W/WN Gate Layers on the wafer surface.

[0042] Cap Nitride

[0043] Figure 2 shows the area after the trench has been etched. A resist 32, shown in Figure 1, has been patterned and top oxide 15 has been etched in an oxide etch.

[0044] Next, a timed reactive ion etch (RIE), performed for exam-

ple in an Applied Materials 5000 tool using conventional chemistry has performed a highly directional etching step down to a level below drains 120, forming trench aperture 210. The chemistry does not attack oxide to any significant degree, so that top oxide 15 serves as a hardmask in this operation. The depth of aperture 210 is nominally enough to get down below the transistor body, compared with the nominal depth of the deep trench in the DRAM cell of 8 microns.

[0045] In operation, current will flow between the body region 130 of the P-well above the drains and the bottom of trench 210 below the drains. The path for the current is completed through the bias supply that biases P-well 20. Thus, the transistor bodies 130 will not be floating, regardless of the length of the depletion regions associated with drains 120.

[0046] Figure 3 shows the area after a number of steps, including: Oxidizing (preferably thermally) the interior surface of trench 210 to a conventional thickness to passivate the surface.

[0047] A liner of nitride (Si_3N_4) is deposited by CVD to a conventional thickness.

[0048] The nitride is etched with a directional RIE step, so that

the material on bottom 212 is selectively removed without substantially affecting the nitride 222 on the vertical surfaces. In the final structure, there will be current flow through the bottom surface 212.

[0049] The trench is filled with resist that is recessed to a nominal depth of the middle of the body of the vertical transistors, denoted with numeral 224.

[0050] The nitride 222 on the interior surface of the trench is stripped above depth 224, illustratively with hot phosphoric acid, to leave the oxide on surfaces 223.

[0051] The resist is stripped and the trench interior is subject to a step of nitridation, in which a gas containing nitrogen that reacts with the material in the trench is introduced at a conventional temperature such that the oxide on surfaces 223 is converted to nitride 226 (or a layer of nitride is deposited) to a nominal thickness. The gas thickens the nitride 222 slightly and deposits a layer 228 at the bottom of trench 210. The nitridation is similar to that done in the buried strap interface and does not hinder conduction significantly, but serves to passivate the silicon in that area.

[0052] The trench is filled with boron-doped poly 227 (doped P^+) that is recessed to a nominal depth above the top of ni-

tride liner 222.

[0053] Subsequent high-temperature steps will diffuse boron into the transistor body regions 130 to establish a relatively low-resistance path from the body 130 to the lower level.

[0054] The presence of the outdiffusion 230 will affect the threshold of the vertical transistors. Preferably, the initial doping of the vertical transistors is set such that the final threshold is correct.

[0055] Figure 5 shows the area after the steps of nitride divot fill, in which a conformal layer of nitride is deposited that fills the top of the contact trenches and also penetrates laterally to fill any "divots" resulting from previous etching steps.

[0056] After conventional chemical-mechanical polishing to remove the excess nitride, a layer of Tungsten Nitride 51 and Tungsten 52, followed by a Nitride cap layer 55 is put down. Layers 51 and 52 will be patterned to form the word lines at any convenient time. The bit lines will also be formed by conventional processes at any convenient time.

[0057] While the invention has been described in terms of a single preferred embodiment, those skilled in the art will

recognize that the invention can be practiced in various versions within the spirit and scope of the following claims.